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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Hoke et al.
Serial No.:	09/504,660
Filed:	February 14, 2000
Entitled:	Double Recessed Transistor
Docket No.:	RTN2-047PUS (formerly 07206/047001)

Group Art Unit: 2811
Examiner: T. Thomas

Certificate of Mailing (37 C.F.R. 1.8(a))

I hereby certify that this correspondence is being transmitted via first-class mail in an envelope Addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on the date set forth below.

_____ By:_____

Date of Signature
and Mail Deposit

DECLARATION UNDER 37 CFR 1.131

Assistant Commissioner for Patents
Washington, D.C. 20231

I, William E. Hoke, state that:

1. I am a co-inventor of the above-identified patent application;

2. I, jointly with Katerina Y. Hur, completed the invention claimed in the above-identified patent application in the United States prior to September 29, 1997.

3. In support thereof, I submit the following evidence:

A. Record of Invention form and disclosure document entitled "High Breakdown Voltage, Strain Compensated $Al_{0.60}In_{0.40}As/Ga_{0.35}In_{0.65}As/InP$ HEMTs" attached EXHIBIT;

B. Said disclosure document states on page 1 of the disclosure document: "We have invented an $Al_{0.60}In_{0.40}As/Ga_{0.35}In_{0.65}As/InP$ HEMT structure ... to simultaneously deliver high output current (690-850 mA/mm) and high breakdown voltages (9-11 V). The new HEMT structure utilizes a strained $Al_{0.60}In_{0.40}As$ Schottky layer and a strained $Ga_{0.35}In_{0.65}As$ channel. ... We call this new HEMT structure a strain compensated HEMT structure due to the fact that the tensile strain in the $Al_{0.60}In_{0.40}As$ Schottky layer is compensated by the compressive strained in the $Ga_{0.35}In_{0.65}As$ channel layer ".

C. Said document states on page 2: "Fig. 2 shows the output current density and reverse gate-to-drain breakdown voltages measured on several double recessed, strain compensated AlInAs/GaInAs/InP HEMTs with variable source-to-drain spacing and first recess width".

D. The table on page 2 is captioned: Fig. 2 Results of DC IV characteristics of double recessed, strain compensated AlInAs/GaInAs/InP HEMT with variable source-to-drain spacing (SD) and first recess width (Lr).

E. As stated on page 1 of the disclosure document: "Fig. 1 shows the new HEMT layer structure. The epitaxial layer structure consists of a heavily doped $Ga_{0.47}In_{0.53}As$ cap layer, an $Al_{0.48}In_{0..52}As$ recess layer, an $Al_{0.60}In_{0.40}As$ Schottky layer, a top Si pulse doped layer, an $Al_{0.48}In_{0.52}As$ spacer, $Ga_{0.35}In_{0.65}As$ channel, an $Al_{0.48}In_{0.52}As$ spacer, a bottom Si pulse doped layer, and an $Al_{0.48}In_{0\cdot52}As$ buffer layer grown on top of the semi-insulating InP substrate".

F. The dates have been removed from the attached copy in Exhibit but on the original said dates are prior to September 29, 1997.

4. All statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true.

5. I understand and have been advised that willful false statements and the like made herein are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon.

William E. Hoke

William E. Hoke

Date: Jan 16, 2002

Re rd Of Invention

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Raytheon

10-5976 (12/99)

An Invention Disclosure should be submitted on every new or improved device, system, method, or composition of matter devised by you, which is more than routine engineering. Prepare three copies of this R cord of Invention Form and sign each copy. Attach to each one your Invention Disclosure. Forward two sets to th Patent Section of th Law Department through your Division Manager via your supervisor, and a third set **directly** to the Patent Section of the Law Department.

The Invention Disclosure should contain:

1. A statement and discussion of the problem solved by the invention.
2. A complete description of the inventive device, system, or method including sketches or drawings, and an explanation of how the invention works and **how it solves the problem.**
3. A brief statement of why you believe the invention to be new. Specifically point out important features believed to be novel. State the advantages of invention and the sacrifices, if any, made to achieve these advantages.
4. State possible commercial and/or military uses of the invention. If the concept of the invention is applicable to other problems and fields of interest, state what they are, and how the principles of the invention would be used.

Inventor(s)	Employee No.	Division	Location
(1) KATERINA V. HUR	90972	AOC RESEARCH	ANDOVER
(2) WILLIAM E. HOKE			
(3)			

Title Of Invention
HIGH BREAKDOWN VOLTAGE, STRAIN COMPENSATED $Al_{.6}In_{.4}As$ / $Ga_{.35}In_{.65}As$ / INP HEM

To Whom First Disclosed? Date
THOMAS E. KAZIOR, LISA M. AUCOIN

Invention Described On Pages | Technical Notebook No. | Date
38619 - 99 | 38619

Names Of Witnesses To Technical Notebook Entry
THOMAS E. KAZIOR, SHIOU-LONG (GRACE) CHU

Was The Invention Built And Successfully Tested? Date
☐ No ☑ Yes ▶ If "Yes", By Whom? B. LeBLANC, R. McTAGGART, K. HUR

Witnesses Of Test (Witnesses Must Be Personally Conversant With Details Of Device Tested, The Test Itself And The Results)
THOMAS E. KAZIOR, SHIOU-LONG (GRACE) CHU

Where Are Test Results Recorded?
POLAROID PICTURES (K. HUR)

Has The Invention Been, Or Is The Invention To Be, Incorporated In A Company Product?
☑ No ☐ Yes ▶ If Yes, Identify Product And Describe Nature Of And Give Date(s) Of Any Release, Promotion, Or Discussion Of The Product Outside Raytheon.

Has The Invention Been Disclosed Outside Raytheon?
☑ No ☐ Yes ▶ If Yes, Identify And Give Date(s) Of The Disclosure.

Does The Invention Relate Directly To Work Done Under Any Company Funded Program (Examples: IDP, IRP, Or Proposal Effort)
☑ No ☐ Yes ▶ If Yes, Identify Specific Program Or Project.

Does The Invention Relate Directly To Work Done Under Any Specific Government Contract?
☐ No ☑ Yes ▶ If Yes, State Contract Number And Security Classification. DSI-300
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Inventor(s) Signature Date

(1) Katerina Hur — Month / Day / Year

(2) William E. Hoke — Month / Day / Year

(3) _____ Month / Day / Year

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High Breakd wn Voltage, Strain Compensated $Al_{0.60}In_{0.40}As/Ga_{0.35}In_{0.65}As$/InP HEMTs

Katerina Y. Hur and William E. Hoke

Raytheon Electronics
Advanced Device Center,
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InP-based HEMTs are attractive devices for use in monolithic millimeter wave integrated circuits due to their record performance in high frequency and low noise characteristics. Despite the significant advancement in low noise applications, InP-based HEMTs have not been fully utilized for high power applications due to their low breakdown voltages (typically less than 6 V).

Previously, a double recessed gate process was developed for AlInAs/GaInAs/InP HEMTs[1] to significantly increase breakdown voltage. However, one problem with the double recessed AlInAs/GaInAs/InP HEMT is low output current (as low as 400 mA/mm). We have invented an $Al_{0.60}In_{0.40}As/Ga_{0.35}In_{0.65}As$/InP HEMT structure compatible with the double recess process to simultaneously deliver high output current (690 - 850 mA/mm) and high breakdown voltages (9 - 11 V). The new HEMT structure utilizes a strained $Al_{0.60}In_{0.40}As$ Schottky layer and a strained $Ga_{0.35}In_{0.65}As$ channel layer. Because of the larger conduction band discontinuity between the Schottky and channel layers, high output currents can be obtained. Low breakdown voltage typically associated with using the $Ga_{0.35}In_{0.65}As$ channel layer (less than 4 V) was significantly enhanced by the use of a double recessed gate process. We call this new HEMT structure a strain compensated HEMT structure due to the fact that the tensile strain in the $Al_{0.60}In_{0.40}As$ Schottky layer is compensated by the compressive strained in the $Ga_{0.35}In_{0.65}As$ channel layer.

Fig. 1 shows the new HEMT layer structure. The epitaxial layer structure consists of a heavily doped $Ga_{0.47}In_{0.53}As$ cap layer, an $Al_{0.48}In_{0.52}As$ recess layer, an $Al_{0.60}In_{0.40}As$ Schottky layer, a top Si pulse doped layer, an $Al_{0.48}In_{0.52}As$ spacer, $Ga_{0.35}In_{0.65}As$ channel, an $Al_{0.48}In_{0.52}As$ spacer, a bottom Si pulse doped layer, and an $Al_{0.48}In_{0.52}As$ buffer layer grown on top of semi-insulating InP substrate. The top to bottom Si pulse ratio was 2.5 to 1.5. Typical carrier sheet density was 4×10^{12} cm^{-2} and Hall mobility was 9600 cm^2/V-sec at room temperature.

The wet etch process for mesa isolation with a channel notch consists of a 20 sec. etch in 1:8:160 H_2SO_4:H_2O_2:H_2O and a 90 sec. etch in 6:1 succinic acid:H_2O_2 etchant.

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[1] K. Y. Hur, et al. 1995 IEEE GaAs IC Symposium

Ohmic contacts for the source and drain pads were fabricated using a 900Å AuGe - 2000Å Au metallurgy and a 375°C alloy furnace. Typical unrecessed saturation current, Isat, was greater than 1000 mA/mm. Electron beam lithography and the 1:1:100 H_3PO_4:H_2O_2:H_2O etchant was used for the first recess and gate etch. For the first recess etch, the wafer was etched until the current level in the range, 0.75 Isat - 0.8 Isat, was reached. After the gate recess etch to a current level in the range, 0.6 Isat - 0.65 Isat, Schottky metal consisting of 500 Å Ti - 500Å Pt - 4000Å Au was deposited and lifted off.

Fig. 2 shows the output current density and reverse gate-to-drain breakdown voltage measured on several double recessed, strain compensated AlInAs/GaInAs/InP HEMTs with variable source-to-drain spacing and first recess width. Maximum output current as high as 850 mA/mm with corresponding breakdown voltage of 9.6 V have been demonstrated. Typical extrinsic transconductance in excess of 600 mS/mm was measured at Vds = 2V. Therefore, the new strain compensated AlInAs/GaInAs/InP HEMT layer structure may be potentially a viable material for microwave and millimeter power MMICs.

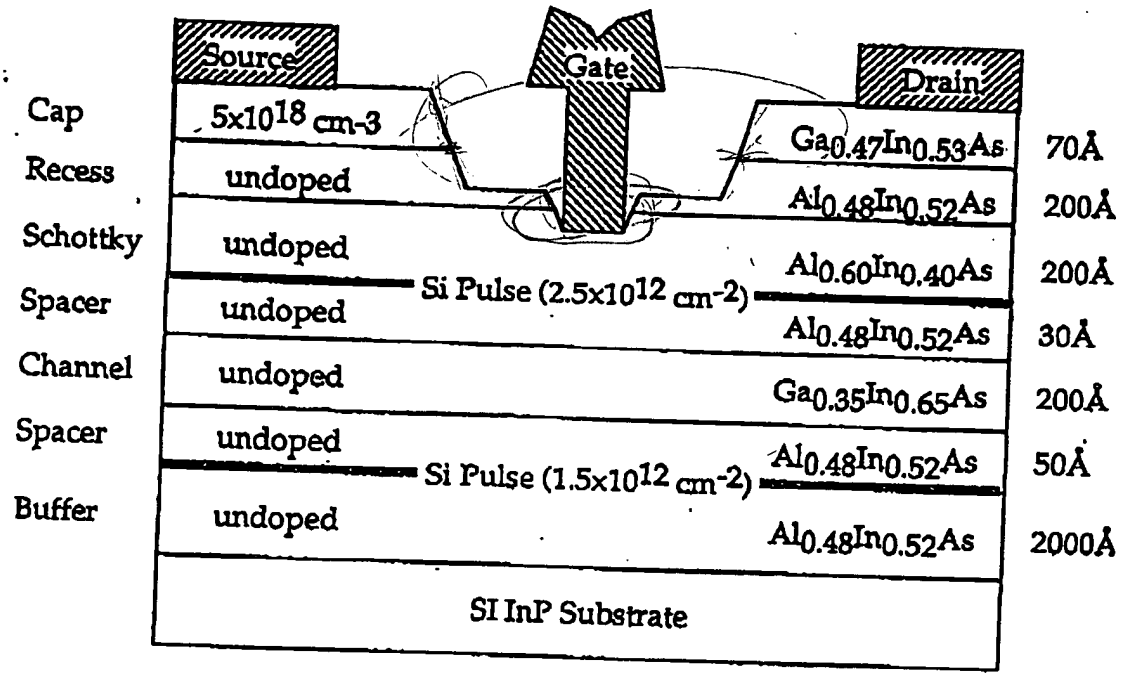

Fig. 1. The layer structure of the double pulse doped, double recessed, strain compensated AlInAs/GaInAs/InP HEMTs.

SD (μm) / Lr (μm)	Imax (mA/mm)	Vbdg (V)
1.8/0.8	846	9.6
2.0/1.2	785	10.6
2.0/0.8	848	9.6
2.2/1.2	764	10.7
2.4/0.8	778	9.7
2.6/1.2	692	11.2

Fig. 2. Results of DC IV characteristics of double recessed, strain compensated AlInAs/GaInAs/InP HEMTs with variable source-to-drain spacing (SD) and first recess width (Lr). Output currents (Imax) in the range 690-850 mA/mm and breakdown voltage (Vbdg) in the range 9-11 V have been obtained.